Exhibit A

BRFile Copy

MAGMA DESIGN AUTOMATION, INC.
5460 Bayfront Plaza | Santa Clara, CA 95054-3601 USA | Tel 408-565-7500 | Fax 408-565-7501 | www.magma-da.com

July 1, 2004

Rex Jackson, Esquire
Vice President and General Counsel
Synopsys, Inc.
700 E. Middlefield Road
Mountain View, CA 94043

Re: Concerns Regarding Synopsys' "Gain-Based Delay Model"

Dear Rex:

This letter is intended to express certain concerns of Magma Design Automation, Inc. ("Magma") with respect to claims made recently by Synopsys that it has implemented a new "gain-based delay model" in an enhanced version of Design Compiler.

We recently noted a posting in ESNUG 430, available at www.deepchip.com. See Item No. 3 "compile_new_optimization Turns On Gain-based Synthesis in DC?" which was posted on June 16, 2004. A user of Design Compiler (from a semiconductor company) quotes the following excerpt from a Synopsys "man-page" (user manual):

"Controls which optimization algorithms Design Compiler uses. When true, the new optimization algorithms in Design Compiler are turned on. This switch should be used in conjunction with the set_ultra_optimization command, which checks out a DC-Ultra license. The new optimization algorithms leverage a new gain-based delay model that is automatically derived using library analysis."

Magma is concerned that Synopsys' new optimization technique may read on one or more of Magma's patents, namely the following:

1. U.S. Patent No. 6,253,361, dated June 6, 26, 2001, entitled "Generalized Theory of Logical Effort for Look-Up Table Based Delay Models Using Capacitance Ratio" ("'361 Patent").

2. U.S. Patent No. 6,453,446 dated September 17, 2002, entitled "Timing Closure Methodology" ("'446 Patent").

3. U.S. Patent No. 6,725,438dated April 20, 2004, entitled "Timing Closure Methodology" ("'438 Patent"), a continuation of the '446 Patent.

Specifically, the '361 Patent describes the method associated with Magma's delay model, which is used to reduce gate delay by adjusting electrical efforts in each stage. The '446 Patent and the '438 Patent describe a method whereby the predetermined delay constraints in this delay model are employed in the context of the timing closure methodology Magma calls FixedTiming (R) – a method which Synopsys has publicly discounted in the past.

The Synopsys man-page quoted by the user in ESNUG suggests that Design Compiler includes a gain-based delay model as taught by the '361 Patent, the '446 Patent and the '438 Patent (collectively, the "Patents").

We trust that Synopsys has no intent to infringe the Patents, copies of which are attached for your reference. We request that Synopsys advise us whether Synopsys believes that one or more of the Patents are applicable to Synopsys' gain-based delay model, or any other Synopsys design solution.

I look forward to your prompt written response.

Sincerely,

Beth Roemer

Beth Roemer
Vice President and General Counsel

cc: Steve Shevick, Chief Financial Officer

Encls